Nicole Lesperance

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Education

- **University of California - Santa Barbara** — Santa Barbara, California
  MS/PhD Program: Electrical and Computer Engineering — *September 2011 – Present*
  - Advisor: Professor Kwang-Ting (Tim) Cheng
  - SoC Design and Test Lab (`http://cadlab.ece.ucsb.edu`)
  - GPA: 4.0
- **The Cooper Union for the Advancement of Science and Art** — New York, New York
  Bachelor of Engineering, Electrical Engineering — *September 2007 – June 2011*
  - GPA: 3.9
  - Full-tuition merit scholarship

Publications

- N. Lesperance, S. Kulkarni, and K-T. Cheng, "Hardware Trojan Detection Using Exhaustive Testing of k-bit Subspaces", Asia South-Pacific Design Automation Conference (ASP-DAC), 2015.
- N. Lesperance, P. Lisherness, and K-T. Cheng, "Coverage Discounting: Improved Testbench Qualification by Combining Mutation Analysis with Functional Coverage", SRC TechCon, 2013.
- P. Lisherness, N. Lesperance, and K-T. Cheng, "Mutation Analysis with Coverage Discounting", Design, Automation Test in Europe (DATE), 2013.
- N. Lesperance, M. Leece, S. Matsumoto, M. Korbel, K. Lei, and Z. Dodds, "PixelLaser: Computing Range from Monocular Texture", Advances in Visual Computing, LNCS 6455, pp. 151-160, 2010.

Work Experience

- **Hardware Verification Engineer – Apple Inc.** — Cupertino, California
  Silicon Engineering Group — *Summer and Fall 2013*
  - Created a SystemVerilog testbench for a large design
  - Responsible for writing random and directed tests
- **Software Security Intern – Cisco Systems** — Knoxville, Tennessee
  Cisco Security and Government Group — *Summer 2012*
  - Created a code fuzzer for Multicast Source Discovery Protocol using the Peach fuzzing framework
  - Completed a series of practical applied security exercises
  - Learned to recognize and remedy common vulnerabilities in C programs

Current Research

- **Hardware Trojans in Unspecified Design Functionality** — UC - Santa Barbara
  - Developing analysis techniques for RTL and SystemC designs to ensure unspecified functionality does not provide opportunity for Trojan insertion
  - Created a Trojan modifying only RTL Don't Cares in an Elliptic Curve Processor (ECP) Verilog design with the ability to leak all key bits
  - Developed prevention methodology based on combinational equivalence checking and validated effectiveness using the ECP design

- **Coverage Discounting** UC - Santa Barbara
  Published at SRC TechCon and DATE in 2013
  - Current research explores using mutation analysis to 1) extend the coverage model and 2) identify unspecified and untested functionality vulnerable to Hardware Trojan insertion
  - Coverage Discounting uses mutation analysis to improve existing coverage metrics by accounting for the effectiveness of error propagation in the test bench
  - Evaluated Discounting technique on the OpenRISC and UART designs from OpenCores
- **Hardware Trojan Detection Using Exhaustive Subspace Testing** UC - Santa Barbara
  Published at ASP-DAC in 2015
  - Developed a post-silicon Hardware Trojan detection strategy based on the observation that an attacker is only able to use a small subset of design signals for Trojan triggering
  - Method targets exhaustive coverage of all possible subsets of signals the attacker could select instead of using controllability and observability metrics to bias testing
  - Evaluated technique on AES core

Projects

- **Design of a Modern Processor and Memory Hierarchy** UC - Santa Barbara
  Advanced Computer Architecture *Winter 2012*
  - Implemented a two-level memory hierarchy shared between 4 processors using behavioral Verilog
  - Implemented a superscalar processor capable of dispatching two instructions per cycle using Tomasulo's algorithm using behavioral Verilog
  - Exception handling implemented by using an instruction reorder buffer
- **PixelLaser: Computing Range from Monocular Texture** Claremont, California
  Harvey Mudd College *Summer 2010*
  - Developed an image segmentation pipeline that analyzes a web-camera image using color and texture descriptors to compute distances to non-traversable terrain
  - Uses the iRobot Create platform controlled by a netbook running Python and OpenCV scripts
  - Implemented applications of range-scans include Monte-Carlo localization and map-building
  - Attended the 2010 AAAI Conference in Atlanta to exhibit the robot

Skills

Programming Languages: C, SystemVerilog, Verilog, C++, Python, Perl, Ruby, Matlab, x86, VHDL, MIPS

Computer Utilities: ModelSim, VCS, Synopsys Design Compiler, Primetime, Matlab, Unix Command Line, GDB, Certitude, ABC Logic Synthesis Tool, Cadence SMV, Xilinx ISE Design Suite, Flex, Bison, OpenCV, LaTeX, Octave, HSPICE

Laboratory Equipment: Oscilloscope, Logic Analyzer, Soldering Iron, Arduino, Raspberry Pi

Activities and Academic Honors

- Selected to teach a seminar on Matlab and also provide supplementary presentation of topics in signal processing and control systems (2010 – 2011)
- Winner of the Leon Machiz Prize for excellence in electrical engineering (2011)
- Winner of the Class of 1907 Award for the best enrolled or graduating student in calculus (2011)
- Winner of the Jesse Sherman Book Award for Outstanding Average in Electrical Engineering (2010, 2011)
- Dean's List at Cooper Union (8 consecutive semesters)