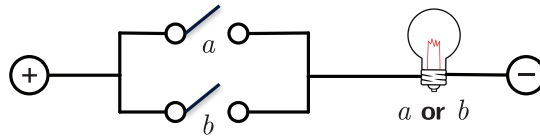(a)

(b)

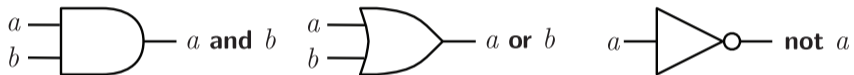Figure 2.1 Simple electrical implementations of an (a) and **and** (b) **or** gate.

002x001.eps

Figure 2.2 Schematic representations of logic gates.

002x002.eps